AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of the claims in the above-captioned patent application.

Listing of Claims:

Claim 1. (Currently Amended) A semiconductor integrated circuit, comprising:

a current generator circuit configured to generate a first current substantially proportional to an absolute temperature, the first current being determined by [[a]] size ratio of [[a]] MOS transistors, and by a resistor; and

a starting-up circuit configured to set said current generator circuit ~~to generate the first current~~ at a stable working point ~~of said current generator circuit~~ in which said current generator circuit generates the first current,

wherein

~~while said current generator circuit operates at the stable working point,~~ a current that flows through said starting-up circuit when said current generator circuit operates at the stable working point is determined by a ~~diffusion~~ resistance and [[a]] MOS transistors connected in series provided in said starting-up circuit.

Claim 2. (Original) The semiconductor integrated circuit as claimed in claim 1, further comprising:

a voltage generator circuit that generates a reference voltage substantially independent of the absolute temperature using the first current generated by said current generator circuit.

Claim 3. (Original) The semiconductor integrated circuit as claimed in claim 2,

wherein

said voltage generator circuit comprises:

one of a bipolar transistor and a diode; and

a resistor connected to said bipolar transistor or said diode; and

said voltage generator generates the reference voltage by flowing a second current proportional to the first current through a series of the one of the bipolar transistor and the diode, and the resistor.

Claim 4. (Currently Amended) A semiconductor integrated circuit, comprising:

a current generator circuit that generates a first current substantially proportional to an absolute temperature; and

a voltage generator circuit that generates a reference voltage substantially independent of the absolute temperature using the first current generated by said current generator circuit,

wherein

said voltage generator circuit comprises:

a first element that generates a voltage that is substantially linearly reduced as the absolute temperature increases;

a resistance division circuit connected in parallel to said first element;

a second element connected to the parallel connection of said first element and said resistance division circuit, wherein said second element provides a second current proportional to the first current; and

a third element connected to a node between resistors of said resistance division circuit, wherein said third element provides a third current proportional to the first current.

Claim 5. (Original) The semiconductor integrated circuit as claimed in claim 4,

wherein

said first element is one of a bipolar transistor and a diode.

Claim 6. (Original) The semiconductor integrated circuit as claimed in claim 4,

wherein

said current generator circuit generates the first current determined by a size ratio of a MOS transistor, and by a resistor.

Claim 7. (Currently Amended) A semiconductor integrated circuit, comprising:

a first NMOS transistor that is provided with a voltage to a gate thereof, which voltage is generated by dividing a power supply voltage with resistors;

a second NMOS transistor that is provided with a reference voltage to a gate thereof;

a first PMOS transistor and a second PMOS transistor diode-connected to each other;

a third PMOS transistor, a gate of which is connected to a gate electrode of said first PMOS transistor;

a fourth PMOS transistor, a gate of which is connected to a gate electrode of said second PMOS transistor;

a third diode-connected NMOS transistor ~~connected as a diode~~;

a fourth NMOS transistor, a gate of which connected to the gate of said third NMOS transistor, and

a first resistor,

wherein

a source electrode of said first NMOS transistor and a source electrode of said second NMOS transistor are connected to each other;

a drain of said first NMOS transistor and a drain of said first PMOS transistor are connected to each other;

a drain of said second NMOS transistor and a drain of said second PMOS transistor are connected to each other;

a drain of said third PMOS transistor and a drain of said third NMOS transistor are connected to each other;

a drain of said fourth PMOS transistor and a drain of said fourth NMOS transistor are connected to each other;

a first end of said first resistor is connected to the power supply voltage;

a second end of said first resistor is connected to the drain of said fourth PMOS transistor and to the drain of said fourth NMOS transistor; and

the semiconductor integrated circuit outputs a voltage of the second end of said first resistor for determining whether the power supply voltage is lower than a predetermined voltage.

Claim 8. (Original) The semiconductor integrated circuit as claimed in claim 7,

wherein

the reference voltage is generated by the semiconductor integrated circuit as claimed in claim 2.

Claim 9. (Currently Amended) A semiconductor integrated circuit, comprising:

a first pnp bipolar transistor;

a second pnp bipolar transistor;

a first resistor connected in series to an emitter of said first pnp bipolar transistor;

a second resistor connected in series to an emitter of said second pnp bipolar transistor;

a third resistor connected in series to an end of said first resistor, resistance of said third resistor is equal to the resistance of the second resistor; and

an operational amplifier that is provided with a voltage generated by level-shifting an emitter voltage of said second pnp bipolar transistor to a positive direction with said second resistor as a first input, and with a voltage generated by level-shifting a voltage at the end of said first resistor to a positive direction with said third resistor as a second input,

wherein

said operational amplifier receives the first input and the second input as a gate input of a differential pair of NMOS transistors, and is negatively fed back so that a voltage of the first input and voltage of the second input are equalized.

Claim 10. (Currently Amended) The semiconductor integrated circuit as claimed in claim 9, further comprising:

a voltage generator circuit that generates a reference voltage substantially independent of an absolute temperature using a first current flowing through said first pnp bipolar transistor,

wherein

said voltage generator circuit further comprises:

a first element that generates a voltage that is substantially linearly reduced as the absolute temperature increases;

a resistance division circuit connected in parallel to said first element;

a second element that provides a second current proportional to the first current, said second element connected in parallel to the parallel connection of said first element and said resistance division circuit; and

a third element that ~~provide~~ provides a third current proportional to the first current, the third element connected to a node between resistors of said resistance division circuit.

Claim 11. (New) The semiconductor integrated circuit as claimed in claim 1, wherein the resistance that determines the current that flows through said starting-up circuit when said current generator circuit operates at the stable working point is a diffusion resistance.